V-quantum machines?

V machines: an invitation to build, run and verify.

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I am not invalidating research in quantum computing. I am proposing an opportunity for construction and comparison: to develop machines that I call V, using electronic logic and conventional programming, to check which problems they solve against the known results of Q machines and with what order of execution.

My proposal is to build non-simulated quantum machines on that conventional foundation. The equivalence being sought must be established through the tasks solved and their order of execution, not through architectural similarity or an answer supplied in advance.

Within the Einstein–VED framework, I place the explanation of prior lack of knowledge and measurement in the temporal function f and in the act of observing at $t=t_0$. Knowing a formula or a connection is not the same as knowing the values of a prepared execution. Measurement fixes what was unknown up to that instant.

I invite researchers and working groups in quantum computing, electronics and programming to build these V machines, respecting their rules, and compare their results. The work provides documents, construction sheets, programs, inputs and tests to do so reproducibly.

Three construction requirements

1. Lack of knowledge before measurement. Undefined inputs and internal states must not be known before the circuit collapses or is read. Values explicitly fixed as 0 or 1 are the exception. We can take $t=0$ as the origin of the measurement event; more generally, we write it as $t=t_0$. Preparing is neither measuring nor assigning outputs in advance.

2. Independence and coherence after preparation. Preparation must ensure the independence of unfixed Qvbits and the lack of knowledge of their values. In my framework, the extent to which that independence is achieved determines the machine's degree of coherence and the reliability of the result. At the same time, the relationships established by the circuit must be preserved: a shared connection is not replaced by different values in each module. Software access tests are not presented as a physical measurement of that independence already performed.

3. Collapse and propagation. Only upon measurement at $t=t_0$ do the unfixed Qvbits become determined in {0,1}. The values propagate through the connections and modules until the output is defined. The trigger is shared: no independent measurements are added during propagation, and a source is not queried again to change its result.

The machines that were run do not incorporate random draws or statistics to produce their outputs. Nor do they use a global register of 2^n states, a bank of Q answers or repetition until a favorable answer is obtained. Comparison takes place outside V, after the measurement has been saved.

What results are available so far

V1 · Deutsch's problem. For the four possible binary functions, the bit that solves the task matches the known Q1 result: $q_0=f(0)\oplus f(1)$. The result is supported by an exact algebraic argument, 16 trials with a controlled trigger and four captures with a real clock. For this fixed two-unit protocol, the core's time and memory are O(1) per execution.

V2 · Obtaining factors through readout and common post-processing. An earlier capture for N=21, base 2, produced the readout 740; the classical post-processing also used in Q2 recovered the factors 3 and 7. In the new direct trial, one capture for N=15 and another for N=21 both produced the readout 28 and did not allow factors to be recovered using that procedure. The reports identify each execution: earlier successes are not mixed with the new captures, and unhelpful outputs are not omitted.

A single unhelpful readout does not establish a general impossibility; an isolated success does not demonstrate general equivalence with Q2 either. The task must be compared using the same success criterion and a declared execution budget.

V3 · Known gate and measurement results. The three cases with determined outputs match their Q references: H followed by H → [0,0,0]. H–RZ(π)–H on the first port → [1,0,0]. RX(π) on the third port → [0,0,1].

In the fourth case, H on the first two ports followed by terminal CZ and RZ gates, the recorded output was [1,0,0], one of the four allowed outputs. This membership check is not confused with demonstrating a complete distribution.

The V3 family with H-H per unit was also run with 2, 8, 32 and 128 units: all outputs were zero, as required by the reference. For this family, traversal and memory are linear at fixed precision. That conclusion is not extended to every V3 circuit.

The 14 rule tests for V2 and V3 checked the blocking of prior reads, a shared trigger, propagation without rereading and the absence of random draws or statistics to generate outputs. The new trials ran the conventional V software directly, without running a Q simulation. Their references are known theoretical results, not Q hardware measurements.

General equivalence of results and orders of execution for V2/Q2 and V3/Q3 remains the objective of the comparison. Quantum hardware timings are not attributed to a software execution, nor is an asymptotic order demonstrated by dividing two isolated timings.

The work and its explanations

Original ES_52 work:
https://estradad.es/teorias/pdf/UNIHOLOG/EN_52_Maquina_V_UNIHOLOG.pdf

Base document in UNIHOLOG:
https://estradad.es/teorias/pdf/UNIHOLOG/EN_52_Maquina_V_UNIHOLOG.pdf

Results, conditions and scope of the tests:
https://estradad.es/teorias/pdf/UNIHOLOG/EN_52_Resultados_preparacion.pdf

Index of documents, programs, construction sheets and supplementary materials:
https://estradad.es/teorias/pdf/UNIHOLOG/EN_52_Indice_recursos.pdf

Construction sheets: https://estradad.es/teorias/pdf/UNIHOLOG/EN_52_Laminas_Q_V.pdf

Translators, compilers and usage:
https://estradad.es/teorias/pdf/UNIHOLOG/EN_52_Traductores_y_compiladores_de_V.pdf

Relationships, measurement and Bell:
https://estradad.es/teorias/pdf/UNIHOLOG/EN_52_Relaciones_medida_y_Bell.pdf

Programs, tests and data

V1: test program and inputs.
https://estradad.es/teorias/pdf/UNIHOLOG/Traductores_V/Pruebas_V/test_v1.py
https://estradad.es/teorias/pdf/UNIHOLOG/Traductores_V/Pruebas_V/data_v1.json

V1: exact argument and established results.
https://estradad.es/teorias/pdf/UNIHOLOG/Traductores_V/Pruebas_V/resultado_asentado_v1.json

V2: composition and Vf module.
https://estradad.es/teorias/pdf/UNIHOLOG/Traductores_V/v2_compuesta.py
https://estradad.es/teorias/pdf/UNIHOLOG/Traductores_V/vf.py

V2: test and inputs. https://estradad.es/teorias/pdf/UNIHOLOG/Traductores_V/Pruebas_V/test_v2.py
https://estradad.es/teorias/pdf/UNIHOLOG/Traductores_V/Pruebas_V/data_v2.json

V3: deferred execution, test and inputs.
https://estradad.es/teorias/pdf/UNIHOLOG/Traductores_V/v3_diferida.py
https://estradad.es/teorias/pdf/UNIHOLOG/Traductores_V/Pruebas_V/test_v3.py
https://estradad.es/teorias/pdf/UNIHOLOG/Traductores_V/Pruebas_V/data_v3.json

Direct trial with known results: program, data and full report.
https://estradad.es/teorias/pdf/UNIHOLOG/Traductores_V/Pruebas_V/ejecutar_tareas_conocidas_v.py
https://estradad.es/teorias/pdf/UNIHOLOG/Traductores_V/Pruebas_V/data_tareas_conocidas_v.json
https://estradad.es/teorias/pdf/UNIHOLOG/Traductores_V/Pruebas_V/resultados_tareas_conocidas_v

Evaluation of the earlier V2 captures:
https://estradad.es/teorias/pdf/UNIHOLOG/Traductores_V/Pruebas_V/comparacion_tareas_v.json

Declared V2 and V3 readout profiles:
https://estradad.es/teorias/pdf/UNIHOLOG/Traductores_V/Pruebas_V/data_v2_compuesta.json
https://estradad.es/teorias/pdf/UNIHOLOG/Traductores_V/Pruebas_V/data_v3_lectura.json

Audit of the construction rules:
https://estradad.es/teorias/pdf/UNIHOLOG/Traductores_V/Pruebas_V/auditoria_reglas_v2_v3.json

An invitation to the community

I am not asking you to accept equivalence in advance. I invite you to build these V machines using electronic logic and conventional programming, respect the preparation and measurement that define them, run the same problems and publish reproducible results, including those that do not match.

The comparison I propose is concrete: the same inputs, the same problem, an explicit success criterion and analysis of the order of execution. It is time to reconsider the quantum domain from this construction possibility too.

Authorship, ethics and license

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